

## Claims

### What is claimed is:

1. A method for reading registers contained in a series of computational units forming a processing pipeline, the method comprising:
  - 5 (a) receiving a read address pointing to one of said registers;
  - (b) determining a first computational unit of said series which contains said one register based on said read address;
  - (c) initiating a timer to count a first delay time corresponding to said first computational unit;
  - 10 (d) asserting a load enable signal corresponding to said first computational unit;
  - (e) said first computational unit transferring first data from said one register specified by said register address onto a read data bus in response to receiving said load enable signal, wherein the read data bus comprises a series of of logic units;
  - (f) reading said first data from the read data bus in response a read enable signal asserted
  - 15 by the timer upon the expiration of the first delay time.
2. The method of claim 1, wherein each of said logic unit comprises a set of parallel gates.
- 20 3. The method of claim 2, wherein said gates are OR gates.
4. The method of claim 1 further comprising repeating (a) through (f) for each register in a subset of said registers contained in said series of computational units.
- 25 5. A system comprising:

a series of computational units forming a computational pipeline, wherein the series of computational units contain a plurality of registers;

a readback bus comprising a plurality of logic units coupled in a series, wherein a first input of each logic unit is coupled to a corresponding one of the computational units;

a timing unit;

a read buffer coupled to an output of the readback bus;

a read control unit coupled to each of the computational units through a corresponding load enable line, wherein the read control unit is configured to (a) receive a read address pointing to one of said registers, (b) determine a first computational unit of said series which contains said one register based on said read address, (c) initiate the timing unit to count a first delay time corresponding to said first computational unit, (d) assert a load enable signal on the load enable line corresponding to said first computational unit;

wherein the first computational unit is configured to transfer first data from said one register onto the read data bus in response to receiving said load enable signal;

wherein the timing unit is configured to assert a read enable signal upon expiration of the first delay timer;

wherein the read buffer is configured capture said first data from the output of the read data bus in response to the read enable signal.

6. The system of claim 5, wherein the logic unit comprises a parallel set of logic gates.

7. The system of claim 6, wherein the logic gates are OR gates.

8. A system for reading register contents from a computational pipeline comprising a plurality of computational units, the system comprising:

a readback bus comprising a plurality of logic units coupled in a series, wherein each of said logic units couples to a corresponding one of the computational units;

a read control unit coupled to each of the computational units through a corresponding load line, wherein the read control unit is configured to assert a load signal on one of the load lines in response to a register request;

wherein each of said computational units is configured to transmit a data value from a selected register onto the readback bus in response to detecting an assertion of the load signal on its corresponding load line.